**CECS 341 - Lab 8**

**“MIPS Instruction Decode Stage”**

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I certify that this submission is my original work

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Lab Report: Lab Assignment 8 - “MIPS Instruction Decode Stage”

1. **Goal:** The goal of this lab is to understand how the MIPS Instruction Decode stage works. The instruction decode stage is used to generate the value of control signals and perform register access.
2. **Steps:**
   1. Step 1: Read over the entire lab and understand the procedure
   2. Step 2: Copy over the code for the sign extender (se16.v)
   3. Step 3: Copy over the code for the control Unit
   4. Step 4: Copy the code for the regfile that was used in Lab 2 and change the width to 32.
   5. Step 5: Copy over the skeleton code for the design file.
   6. Step 6: Copy over the skeleton code for the test bench.
   7. Step 7: understand what is needed to complete the test bench.
   8. Step 8: Complete the skeleton code for the test bench and complete the Table.
   9. Step 9: Understand how the design module works and complete the skeleton code.
   10. Step 10: Check the answers with the answers provided.
3. **Results:** There are a total of 8 test cases that will go over add, sub, slt, and, or, beq, lw, sw. Each test case has the operation that is being performed and the instruction required to complete that operation. Using test case 0 as an example. The way to find the instruction is to break it into binary. For an rtype instruction, the op code is 000000, rs = 00011, rt = 00100, rd = 00101, sign extend = 00000, and the function code = 100000. When you convert to hex you get, 0x00642820. This then is sent to the modules and the output of the lab is the flags and signals that are on (1), off (0), or doesn’t matter (x).

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| Test Case | Operation | Instruction |
| 0 | Add $5, $3, $4 | 32’h00642820 |
| 1 | Sub $8, $4, $5 | 32'h00854022 |
| 2 | Slt $9, $4, $5 | 32'h0085402A |
| 3 | Beq $10, $4, 2 | 32'h11440002 |
| 4 | Lw $11, 4($0) | 32'h8C0B0004 |
| 5 | Sw $12, 4($0) | 32'hAC0C0004 |
| 6 | And $13, $4, $5 | 32'h00856824 |
| 7 | Or $14, $4, $5 | 32'h00857025 |

1. **Conclusion:** In the is lab I have learned how the MIPS Instruction Decode stage works in the single cycle processor. The challenging part of the lab was understanding how each signal for each input and output worked for each module and determining how the test bench was set up.